MatrixRF:

High-performance heterogeneous SDR platform for 5G MIMO prototype & testing
Since 2008, V3 Technology has been committed to providing high-performance programmable software defined radio system. Through powerful and flexible standardized modules or product combinations, helping scientists and engineers in wireless to quickly realize the algorithm prototype and challenges the innovation limit.

V3 is the certified design partner and authorized training partner of Xilinx, as well as the Chinese partner of ADI. At the same time, we are also provider of IBM Research and Microsoft Research.
Product Lines

Multi-channel & Large-bandwidth Synchronization System
Design for Massive MIMO, phase-array Radar, Channel Simulator & RF Record and Playback

5G Prototype & Testing System
Design for 5G BaseStation & Terminal R&D, 5G algorithm verification and development, 5G product automation test and 5G Education and Research

Open Source SDR
Design for radio hobbyists and engineers, provide open source design platform, support popular development tools, and meet the needs of innovative design.
New Requirements

5G Massive MIMO:
- Multichannel synchronization and automatic calibration technology
- High performance real-time signal processing

Phase-array Radar:
- GHz ultra-bandwidth and mmWave Band
- High RF channel density and support multiple devices combinations

Large-scale Channel Simulation:
- Large scale field programmable gate array (FPGA)
- Flexible and friendly development environment
- Heterogeneous scalable architecture
MatrixRF can realize highly scalable RF channel combination, from the minimum 2T2R to the maximum 128T128R, with real-time bandwidth up to 1GHz and frequency band covering DC to 60GHz millimeter wave. Transmit power and antenna array can be customized according to customer requirements.
Development Flows

Algorithm Engineer:
- MATLAB
- Simulink
- GNU Radio
- LabVIEW

Software Engineer:
- C/C++
- C#
- Python

Hardware Engineer:
- Vivado
MatrixRF System Architecture

PRU
Programmable Radio Unit

PAC
Programmable Accelerator card

PAS
Programmable Algorithm Server
PRU: Programmable Radio Unit

The main function is to complete the digitization of RF and communicate with PAC through high-speed optical fiber interface (40G/100G).

PRU has 3 models: PRU4, PRU6, and PRU8.

- **PRU4**: Cover 30MHz~6GHz, Real-time Bandwidth 200MHz, RF Channel 4Tx/4Rx, 40G SFP+, PCIe2.0 x4 Cable
- **PRU6**: Cover 30MHz~6GHz, Real-time Bandwidth 200MHz, RF Channel 6Tx/6Rx, Dual 40G SFP+
- **PRU8**: Cover DC~4GHz, Real-time Bandwidth 1GHz, RF Channel 8Tx/8Rx, Dual 100G SFP+
PAC: Programmable Accelerator Card

The main function is real-time signal processing, communication with PRU through high-speed optical fiber interface (40G / 100G), and data interaction with CPU through PCIe 3.0x16.

PAC has 2 models: PAC-9P & PAC-5U

<table>
<thead>
<tr>
<th>Factor</th>
<th>PAC-9P</th>
<th>PAC-5U</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA</td>
<td>Xilinx Ultrascale+ 16nm VU9P</td>
<td>Xilinx Ultrascale+ 16nm VU35P</td>
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<tr>
<td>PCIe</td>
<td>PCIe3.0×16/PCie4.0×8</td>
<td>PCIe3.0 × 16/PCie4.0x8/CCIX</td>
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<td>Memory</td>
<td>4*DDR4 DIMM 16GB/32GB 2133MHz 64-bit SDRAM ECC</td>
<td>HBM2 8GB, up to 316GB/s</td>
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<td>Network</td>
<td>2*QSFP28 100GE/40GE</td>
<td>1*QSFP 100GE/40GE</td>
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<tr>
<td>Power</td>
<td>200W</td>
<td>75W</td>
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<tr>
<td>Temp. Range</td>
<td>0℃~45℃</td>
<td>0℃~45℃</td>
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</tbody>
</table>
PAS: Programmable Algorithm Server

The programmable algorithm server is used for the realization of complex algorithm. It interacts with PAC through pcie3.0 interface.

PAS provides 2 configuration options for different application scenarios:
- PAS-5UG based on Core CPU and PAS-2US based on Xeon CPU

- **PAS-5UG**: 5U height, based on Intel Core i9 processor, with the highest frequency up to 5GHz, for high frequency algorithm requirements.

- **PAS-2US**: 2U high, based on Intel scalable Xeon processor, with a maximum of 56 cores and 112 threads, which is oriented to multi-core algorithm requirements.
Key Technology

- **RF channel phase calibration:**
  Support manual and automatic calibration mode. After phase calibration, the phase error of each RF channel is within 0.05 radian (3 degrees).

- **Distributed clock synchronization:**
  It supports GPS timing synchronization and White Rabbit high-precision synchronization to achieve nanosecond synchronization accuracy.

- **High integration RF front end:**
  The latest broadband RF transceiver adrv9009 and Xilinx innovative rfsoc to realize large-scale, ultra wideband and high integration synchronous RF unit.

- **Latest architecture processor:**
  Xilinx's latest 16 nm Virtex Ultrascale+ FPGA, which can support the latest large bandwidth HBM2 on-chip memory, and realizing algorithm acceleration through pcie4.0 and Intel’s latest architecture core i9 or scalable Xeon CPU.
Typical Application

1. Multi-Channels RF Recording & Playback
2. 5G Massive MIMO System
3. Radar Signal Generator
4. Channel Simulation
5G eMBB Solution based on MatrixRF

Under the condition of 100MHz bandwidth of 2x2 MIMO, the downlink data rates is up to 800Mbps at MCS27.
5G uRLLC Solution based on MatrixRF

Under the condition of 40MHz bandwidth of two antennas, the measured end-to-end delay of the system is less than **1ms**, and the reliability is over **99.999%**.

- 5G uRLLC Features:
  - TDD & FDD
  - 5G Numerology
    - SCS: 60kHZ
    - TTI: 125us
  - 2T2R
  - Bandwidth: 5/10/20/40/80/100MHz
  - 3.5GHz (23dBm) / Sub6GHz(0dBm)/ 5.8GHz (23dBm)

- System Solution:
  - 5G uRLLC BS + 5G uRLLC Terminal = 5G uRLLC Platform
Training

Provide 5G related training and consulting services for customized requirement
Typical Training Customers

- ERICSSON
- Microsoft
- HUAWEI
- ZTE
- SAMSUNG
- NOKIA
- IBM
Thanks

For More Information, Please Log on V3 Website

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