5G General Hardware Platform

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Preface

Universal Platform for Baseband Unit (BBU)

Physical layer solution based on FPGA

Universal Platform for Remote Radio Unit (RRU)

Universal Platform for SW/RHUB
The different performance requirement for 5G in three typical application scenarios

- Massive Machine-Type Communications (mMTC)
  - Ultra-low energy: 10+ years of battery life
  - Ultra-low complexity: 10s of bits per second
  - Ultra-low complexity: 1 million nodes per km²
- Enhanced Mobile Broadband (eMBB)
  - Extreme capacity: 10 Tbps per km²
- Ultra-Reliable Low Latency Communication (uRLLC)
  - Extreme data rates: Multi-Gbps peak rates; 100+ Mbps user experienced rates
  - Deep awareness: Discovery and optimization
  - Extreme user mobility: Up to 500 km/h

Deep coverage
To reach challenging locations

Strong security
e.g., Health / government / financial trusted

Ultra-high reliability
< 10⁻⁵ per 1 millisecond

Ultra-low latency
As low as 1 millisecond

Mission-critical control
A myriad of proposed solutions and technologies to meet the challenges of 5G.

- Cloud-based radio access networks, or virtualized RAN
- More advanced solutions in multiple access and coding/modulation schemes
- New baseband and RF architectures
- New beamforming techniques
- Advanced RF domain processing for efficient and flexible use of spectrum
We provide the solution of general hardware platform to help designers to develop and verify their 5G applications.

- Support full band RRU below 6GHz
- Support cell with 2T2R/4T4R
- Support PA from 2W to 100W
- High efficiency/Flexible/scalable
- Provide L1 solution based on FPGA
The BBU Platform based on the Intel X86 general purposed processors, perform L1/L2/L3 function processing for 5G RAN
UNIVERSAL PLATFORM FOR BASEBAND UNIT (BBU)

Hardware Specifications

- **MEMORY**: 16GB DDR4, 2400M
- **SATA SSD**: 16GB
- **CLOCK**: GPS or OCXO, 1588v2
- **SFP28**
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- **CPU**: Intel X86, 16 cores, 2.0GHz
- **FPGA1**: Xilinx ZU21DR, PS memory: 2GB DDR4, 2400M, PL memory: 2GB DDR4, 2400M
- **FPGA2**: Xilinx ZU21DR, PS memory: 2GB DDR4, 2400M, PL memory: 2GB DDR4, 2400M
- **FPGA3**: Xilinx VU9P, memory: 6GB DDR4, 2400M

PCIe 3.0, X4
SGMII X1
25G Arura X8

SGMII X1
PCIe 3.0, X4
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SGMII X1
PCIe 3.0, X4

Supported verifications of 5G functions

• Flexible CU/DU partition in C-RAN architecture.
• Flexible PHY layer and high layers split between the BBU and RRU.
• Emerging SDN/NFV network infrastructure.
• Delivering the dynamic balance of hardware/software processing.
• Integrated Soft-Decision Forward Error Correction (SD-FEC) hardware cores.
• LDPC codec (SD-FEC) to meet 5G standards and support for custom codes.
• Flexible, high performance connectivity for 10G eCPRI/GbE and expansion into 16G & 25G CPRI in fronthaul.
Supported verifications of 5G functions

- Signal/packet processing hardware accelerators in backhaul.
- 10GbE and expansion into 25GbE in backhaul.
- uWave wireless backhaul and fronthaul with radio card.
- Physical layer and high layers workload acceleration.
- Mobile Edge Computing (MEC) functions.
We can provide the whole solution for physical layer as the roadmap.

- **2019.12**: PBCH, PDCCH
- **2020.3**: PRACH, PDSCH
- **2020.5**: PUCCH, PUSCH
The RRU platform along with the BBU platform above, comprise of a complete verification platform for 5G applications.
**UNIVERSAL PLATFORM FOR REMOTE RADIO UNIT (RRU)**

**Specification**

- **DDR**
  - DDR3/DDR4 2GB

- **OS**
  - Linux

- **CPU**
  - ARM9/
  - ARM contex
  - A53(SOCs)

- **FPGA**
  - Xilinx KU3P / ZU6CG

- **RF Module**
  - BAND: all band below 6G
  - Output power: 33 dBm/antenna
  - Support DPD
  - High power: PA (40W-100W)
  - RF bandwidth: 100M, 200M
  - MIMO: 4T4R/2T2R
Functions

• L1 partial beamforming to reduce fronthaul throughput to baseband

• Flexible 10GbE/eCPRI expansion to 16 or 25Gb CPRI fronthaul

• Radio Digital Front-End (DFE) includes:
  - Digital Up Conversion (DUC)
  - Digital Down Conversion (DDC)
  - Crest Factor Reduction (CFR)
  - Digital Pre-Distortion (DPD)

• Flexible L1 and high layers partitions along with BBU platform.

• TDD and FDD support.

• CPRI IQ Compress/Decompress.

• L1 Offload and acceleration.
Universal Platform for SW/RHUB

SW/RHUB used to converge and distribute the data between BBU and RRU.
Universal Platform for **SW/RHUB**

**Specification**

- **OS**
  - Linux

- **FPGA**
  - Xilinx KU3P / ZU6CG

- **CPU**
  - ARM9

**INTERFACE**

- Uplink/Downlink
  - 2*25G SFP28

- CPRI/eCPRI
  - 10G *8

- Monitor
  - 1*RJ45

- Power
  - DC-48V*8
Universal Platform for SW/RHUB

Functions

• Support cell merging/splitting, data compression/decompression, broadcast/aggregation and low physical layer function.

• Support two levels of cascading

• 2 interface with 25GbE (connect to BBU and cascaded SW)

• 8 optical module interface with 10Gb connect to at least 8 RRU.

• Support photoelectric hybrid cable/POE power to RRU
Etern’s hardware platforms offer an ideal platform to realize split Layer 1 processing, flexible eCPRI/CPRI connectivity and the whole physical layer solution based on the FPGA for virtualized network functions in the baseband pool of 5G C-RAN applications.
THANK YOU!