High Performance Baseband Processor and LTE/LTE-A System Solution

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INTRODUCTION OF HIGH PERFORMANCE BASEBAND PROCESSOR - MAPU
Algebraic Processor MaPU Introduction

- 800MHz ARM Core
- 1.2GHz APE Core
- 40nm LP Process
- Size: 42mmx42mm
- Peak Computational Performance: 768GOPS@16bit

Power:
- Typical 5V, 2.5A.
- 3W for Single Core FFT Instruction
MaPU Novel Conception

- Combine with GP CPU, ASIC and FPGA merits

**Break Computing Bound**
- GP CPU/DSP
  - Programming, Flexible
- IS Based Design

**Break Memory Bound**
- Concentric Circles Model
- Innovative Multi-granularity Parallel Memory

**MaPU**
- Data-Intensive Computing
- Hardware Computing

**ASIC**
- Ordered by Algorithms, High Performance and Low Power

**FPGA**
- Parallel Computing and Memory, reconfigurable
Novel Instruction Set Architecture (ISA) of MaPU

AppAISArc™:

Application Algorithm Instruction Set Architecture™

ISA

• Hard: Micro opts direct control cores
• Soft: Micro opts array pipeline support multiple algorithm

MaPU Pipeline

• bottom level Microcode Pipeline reach ASIC efficiency
• Top level Scalar pipeline support multiple application instructions
MaPU in Mobile Network Advantages

MaPU SOC architecture and Mobile Com Instruction Set provide ultra high computing power (307.2GFLOPS).

Multi-protocol SDR platform, smoothly evolved, software upgrade
# MaPU in Mobile Network Advantages

## MaPU Merits in Mobile eNB Baseband

### Powerful algebra computing

<table>
<thead>
<tr>
<th>Comp Unit</th>
<th>Alg. Comp</th>
<th>Tp Alg Opt</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixed ALU</td>
<td>Vector Add</td>
<td>FFT</td>
</tr>
<tr>
<td>Fixed MAC</td>
<td>Vector Mux</td>
<td>2D Filter</td>
</tr>
<tr>
<td>Single ALU</td>
<td>Matrix Add</td>
<td></td>
</tr>
<tr>
<td>Single MAC</td>
<td>Matrix Mux</td>
<td></td>
</tr>
<tr>
<td>Double ALU</td>
<td>Matrix Trans</td>
<td></td>
</tr>
<tr>
<td>Double MAC</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### LTEPHY

- OFDM
- Chn Est.
- Sync
- Scr/De-Scr
- Pre-coding
- MIMO
MaPU in Mobile Network Advantages

MaPU Merits in Mobile eNB Baseband

Novel “Concentric Circle” Model
- Core
- Reg Stk
- SOC Mem
- DDR

Space Time Conception
- Data Layer Parallel
- Tasks Layer Parallel
- Algorithm Parallel
- User Layer Parallel

LTE PHY Layer Example
- Chn Encode/Decode
- Scrb/DeScrb
- Mod/DeMod
- Chn Est.
MaPU in Mobile Network Advantages

MaPU Merits in Mobile eNB Baseband

Novel AppAISArc™ ISA

- Std Processor: Single Instruction Single Op
- SIMD/VLIW Processor: Multi IS Parallel Ops

ISA Level Low
MaPU in Mobile Network Advantages

MaPU Merits in Mobile eNB Baseband

Novel AppAISArc™ IS

Novel MaPU processor:
CompaOpt for Complex Algorithm

Microcode High Level
Single MC multi tasks

Scrbb
Mod
MaPU key features in Wireless Comms

MaPU Merits in Mobile eNB Baseband

**Strong Algebra Computing Power**

**Novel “Concentric Circle” Model**

**Novel AppAISArc™ ISA**

The novel MaPU architecture provides great **Flexibility**, **performance** and **energy efficiency**, similar to **ASIC**. It provides a powerful guarantee for **Realtime** and **High throughput** of wireless communication systems.
Towards 2020 processors’ Roadmap

极光-C1.0
（Towards 5G wireless communications, 2017, 28nm）

极光-HPP1.0
（Super computing, 2017, 16nm）

极光-M1.0
（Multimedia, 2017, 28nm）

MaPU
(2015, 40nm)

Novel Processor Design Platform with Independent Intellectual property

AppAISArc™ ISA
Design Tools
Manufacturing Tech
Test & Verify
极光-JiGuang-C1.0：Towards 5G

- **极光-C1.0**
  - ARM x 1 + UCP Core x 8

- **UCP Core performance**
  - 1.2GHz
  - 1843.2GOPS@16bit

- 28nm process
- Share memory：192Mb
- Telcoms coprocessor CSCP
- SRIO、PCIe、CPRI
- power < 8W
**JiGuang-C1.0 Advantage**

**Powerful Computation:**
- Broad Band Communications
- Multimedia
- Massive connections

**High reliability and Security:**
- Independent intellectual technology
- National Security,
Commercial Confidentiality,
Personal privacy

**System total solution:**
- Support LTE/LTE-A、WiFi etc.
- Support MIMO、CA、CoMP
HIGH PERFORMANCE LTE/LTE-A BASEBAND SOLUTION Based On MaPU
LTE flat network framework

- **EPS (framework evolution)**
- **EPC (wireless access network evolution)**

- **Uu**
- **X2**

- **MME / S-GW**
- **S1**

- **Mobility Management**
- **Serving Gateway**

- **Ports between MME/SGW eNode B** (TS-36.411, 412, 413, 414)

- **Ports between eNode B** (TS 36.421, 422, 423, 424)

- **EPS**: Evolved Packet System (演进型分组系统)
- **EPC**: Evolved Packet Core (演进型分组核心网)
- **E-UTRAN**: UMTS Terrestrial Radio Access Network
- **UMTS**: Universal Mobile Telecom System

**MaPU**

**RNC**: Radio Network Controller （无线网络控制器—仅3G）
Solution of LTE software base station based on MaPU

Reference System

Simulator Prototype System

Compiling Processing

2*2MIMO 系统可以传输 4 幅 1080p 视频；
1*2MIMO 系统最高支持 2 幅 1080p 视频。
LTE Demo system based on MaPU

- **Performance:**
  supporting 2x2 MIMO
  peak data rate: 150Mbps

- **Development goal:**
  data transmitting and receiving of LTE PUSCH based on MaPU
Prototype system of LTE software base station based on simulator

MaPU source code

code resolving

precoding

database generating

scheduling code generating

parameter delivering code generating

latter compiling

program releasing

ARM simulator

APE simulator

UART terminal

MaPU source code

code resolving

precoding

database generating

scheduling code generating

parameter delivering code generating

latter compiling

program releasing
Rx Processing of LTE/LTE-A PUSCH

UL received signal processing procedure
Rx Processing of LTE/LTE-A PUSCH

<table>
<thead>
<tr>
<th>MODULE</th>
<th>FUNCTION</th>
<th>SPU CLOCK</th>
<th>MPU CLOCK</th>
<th>TOTAL CLOCK</th>
<th>TIME(us)</th>
</tr>
</thead>
<tbody>
<tr>
<td>De-OFDM</td>
<td>UL.RecvFFT</td>
<td>43248</td>
<td>44184</td>
<td>87432</td>
<td>145.72</td>
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<tr>
<td>Resource Demap</td>
<td>UL.RecvRscDeMap</td>
<td>9652</td>
<td>2716</td>
<td>12268</td>
<td>20.45</td>
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<tr>
<td>Channel Estimation</td>
<td>UL.RecvChanEst</td>
<td>6555</td>
<td>8494</td>
<td>15049</td>
<td>25.08</td>
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<tr>
<td>Channel Equalization</td>
<td>UL.RecvMIMO</td>
<td>374</td>
<td>10721</td>
<td>11095</td>
<td>18.49</td>
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<tr>
<td>De-Precoding</td>
<td>UL.RecvDFT</td>
<td>2173</td>
<td>16711</td>
<td>18884</td>
<td>31.47</td>
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<tr>
<td>Demodulation &amp; Descramble</td>
<td>UL.RecvDeModScr</td>
<td>5399</td>
<td>5659</td>
<td>11058</td>
<td>18.43</td>
</tr>
<tr>
<td>Deinterleaver</td>
<td>UL.RecvDeinterleaver</td>
<td>16791</td>
<td>10444</td>
<td>27235</td>
<td>45.39</td>
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<tr>
<td>Rate Dematch</td>
<td>UL.RecvDeRM</td>
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<td></td>
<td></td>
<td></td>
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<tr>
<td>Turbo Decoder</td>
<td>Turbo_decoder</td>
<td>58784</td>
<td>213655</td>
<td>272439</td>
<td>454.07</td>
</tr>
</tbody>
</table>

Total: 455460 us

Algebraic instruction processing time duty ratio

- De-OFDM: 19%
- Resource Demap: 3%
- Channel Estimation: 3%
- Channel Equalization: 3%
- De-Precoding: 6%
- Demodulation & Descramble: 60%
- Deinterleaver & Rate Dematch: 6%
- Turbo Decoder: 2%
## Algebraic instruction performance

**2048 fixed point FFT algebraic instruction**

<table>
<thead>
<tr>
<th>Processor</th>
<th>Unit</th>
<th>Throughput/Msps</th>
</tr>
</thead>
<tbody>
<tr>
<td>MaPU</td>
<td>APE core</td>
<td>1168</td>
</tr>
<tr>
<td>TMS320C6670</td>
<td>FFTC</td>
<td>431</td>
</tr>
</tbody>
</table>

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<tr>
<th>Processor</th>
<th>Unit</th>
<th>Throughput/Mbps</th>
</tr>
</thead>
<tbody>
<tr>
<td>MaPU</td>
<td>Turbo decoder</td>
<td>496</td>
</tr>
<tr>
<td>TMS320C6670</td>
<td>TCP3d</td>
<td>348</td>
</tr>
</tbody>
</table>

![Bar charts comparing MaPU-APE and 6670-FFTC throughput](chart1.png)

![Bar charts comparing MaPU Turbo decoder and TCP3d throughput](chart2.png)
Algebraic instruction performance

MaPU与TMS320C6670加速比统计

<table>
<thead>
<tr>
<th>Category</th>
<th>Acceleration</th>
</tr>
</thead>
<tbody>
<tr>
<td>FFT</td>
<td>8.47</td>
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<tr>
<td>MMSE CE</td>
<td>0.74</td>
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<tr>
<td>DeMod&amp;DeScrb</td>
<td>22.96</td>
</tr>
<tr>
<td>Equ</td>
<td>28.12</td>
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<tr>
<td>CE Linear Int.</td>
<td>37.17</td>
</tr>
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谢谢！