USRP Update

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USRP N320 and N321

- Two modes of operation:
  - Stand-alone (embedded) operation
  - Host-based (network streaming) operation
- Discrete RF front-end (not based on AD9371 as with N300/N310)
- 2x2 Channels (2 Tx and 2 Rx)
- Maximum 200 MHz of instantaneous bandwidth per channel
- Expanded frequency tuning range from 3 MHz to 6 GHz
USRP N320 and N321

- Improved LO sharing
  - Easier to build large phase-coherent MIMO systems
- N320 and N321 both have the ability to import Tx and Rx LOs
- N321 has ability to export Tx and Rx LOs
  - Can act as a master LO source
USRP N320 and N321

- Xilinx Zynq 7100 with dual-core ARM Cortex A9 866 MHz CPU
- Two SFP+ ports and one QSFP+ port for full-rate sample streaming
- RJ-45 port (1 Gbps Ethernet) for remote management capability
- Independent 10 MHz clock and 1 PPS time references
- Includes internal GPSDO and supports White Rabbit synchronization
- Master Clock Rates of 200, 245.76, 250 MHz
- 14-bit ADC, 16-bit DAC
## USRP FPGA Resources

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<th>Zynq 7020 (E310)</th>
<th>Zynq 7035 (N300)</th>
<th>Zynq 7045 (E320)</th>
<th>Zynq 7100 (N310/N32x)</th>
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<td>85K</td>
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<td>350K</td>
<td>444K</td>
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<td>BRAM (MB)</td>
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USRP N320 Photo
USRP N321 Photo
USRP N320 and N321 Photos
USRP N320 Front Panel
USRP N320 Rear Panel
USRP N321 Front Panel
USRP N321 Rear Panel
N320 – 2 Rx @ 250 Msps per channel with RFNoC Fosphor (500 MHz real-time capture bandwidth)
N320+N321 - 4 Rx @ 250 Msps per channel with RFNoC Fosphor (1 GHz real-time capture bandwidth)
White Rabbit (Ethernet Synchronization)

- White Rabbit was developed at CERN
- Ethernet-based network for accurate time transfer and time distribution
- Aimed at geographically-distributed systems and GPS-denied environments
- Suitable for indoor environments and areas with limited GPS coverage
- Based on IEEE 1588 / Precision Time Protocol (PTP) and Synchronous Ethernet (SyncE)
White Rabbit (Ethernet Synchronization)

- Provides sub-nanosecond skew, and sub-picosecond jitter
- Meets synchronization and timing requirements for cellular and other time-sensitive applications
- Supports connections of up to 10 km
- Scalable beyond 1000 nodes
- Open-standard and open-source implementations available
- Alternative to 10 MHz/PPS-based and GPS-based approaches
- Supported on the USRP N300, N310, N320, N321
White Rabbit (Ethernet Synchronization)

- WR-supported SFP modules, network equipment, and single mode fiber required
- Uses dedicated SFP on USRP – Independent SFP ports required for timing and I/Q data
- Seven Solutions (https://www.sevensols.com) is preferred vendor
- WR Switch:
  - https://www.ohwr.org/projects/white-rabbit/wiki/switch
- WR SFP:
USRP 2974

- Equivalent to:
  - USRP X310
  - Two UBX-160
  - GPSDO
  - Intel System-on-Module (SoM)

- Intel SoM specifications:
  - Intel Core i7-6822EQ CPU (2 GHz quad-core)
  - 16 GB DDR4 memory, 512 GB NVMe SSD storage

- Provides stand-alone operation
- Rack-mountable, half-wide 2U form factor
USRP 2974 Photo
USRP 2974 Front Panel
**DPDK**

- Data Plane Development Kit (DPDK)
- Provides a userspace framework to accelerate packet processing
- Reduces packet latency and CPU loading
- Open-source (BSD license)
- Runs under Linux on both Intel x86 and ARM
- Created by Intel in 2010, part of Linux Foundation since 2017
- Widespread hardware support for many network cards
  - Intel, Mellanox, Marvell, Cavium, Chelsio, etc.
DPDK

- UHD specifically requires DPDK version 17.11
- The DPDK API changes between releases
- Tested under Ubuntu 18.04 and Fedora 28
- Should also run with Ubuntu 19.04 and Fedora 30
- UHD version 3.14.1.0 supports DPDK with: X300, X310, N300, N310, N320, N321, E320
- Example configuration:
  - Running 2x2 full duplex at 250 Msp/s per channel with a single N320, using DPDK with 10 Gbps Ethernet card and Intel i9-9900x CPU
Thank you!

Questions?